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Patentanmeldung Nr. Patent application No. Demande de brevet n°

03104627.9

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Koninklijke Philips Electronics N.V.
Groenewoudseweg 1
5621 BA Eindhoven
PAYS-BAS

Bezeichnung der Erfindung/Title of the invention/Titre de l'invention:
(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
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Data communication using constant total current

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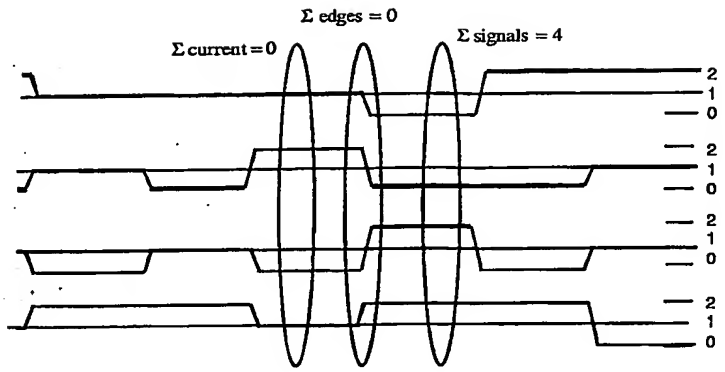

Figure 1

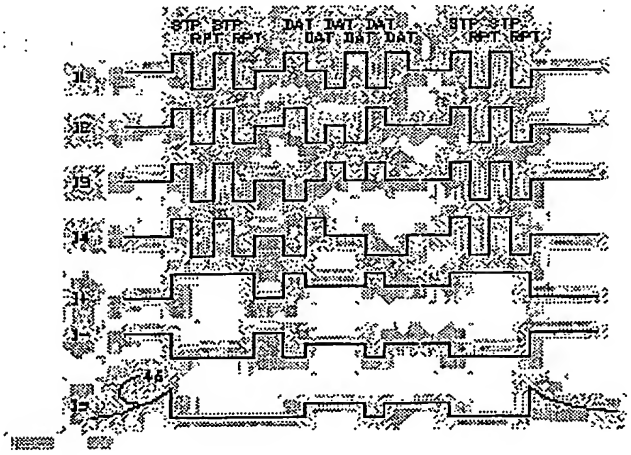

Figure 2

Data communication using constant total current

The invention relates to a data communication system and a method of communicating data.

Such a data communication system is disclosed in US patent No. 6,005,895. The communication system of US patent No. 6,005,895 has the disadvantage that a large number of different levels is needed to provide a large code capacity. To be able to distinguish such currents these currents have to include fairly large currents, which increase power supply consumption. Furthermore a large number of comparisons is needed to decode symbols.

Among others, it is an object of the invention to provide for a large number of different symbols in a communication system, requiring less power consumption to distinguishable different symbols, while keeping the code balanced.

To this end the invention provides a data communication system as defined in the opening paragraph which is characterized by the characterizing features of claim 1.

A method of communicating data as defined in the opening paragraph is characterized by the characterizing features of claim 2.

The above and other objects and features of the present invention will become more apparent from the following detailed description considered in connection with the accompanying drawings in which:

Fig. 1 shows a signal data representation;

Fig. 2 shows an example of data occurring with the I2Q interface, including idle mode. Js indicates the total supply current.

In these figures identical parts are identified with identical references.

Introduction

4 bits binary to 4 bits ternary (Inter IC Quad wire bus: I^2Q) is a bi-directional bus and/or chip-to-chip signaling protocol that is designed from the beginning for speed, an optimal EMC performance by enforcing constant current and moderate power consumption. It derives from five fundamental principles:

a. Maximum performance requires that both near- and far-end reflection coefficients be minimized. Therefore, both near and far-end impedances must closely match the line impedance.

b. The sum of the signals transferred is constant. The data representation is a combination of differential and balanced coding. As such, the sum of currents transferred between the ICs is ZERO, resulting in minimal ground and peripheral supply bounce.

c. For reasonable power consumption and sufficient noise margin, the signal swing should be as small as is consistent with receiver performance. The minimum swing needed for receiver performance shall be the V_T voltage of the input transistors used plus the required noise margin as minimum. As a result, the signaling protocol is independent of the positive supply.

d. An integrated small reference (band-gap) voltage, V_{TT}, shall used be fixed to commonly half the peripheral supply voltage and therefore peripheral supply voltage independent.

e. With the differential signals and the balanced coding, the two spare codes are used to allow synchronization of the clock recovery circuitry at the receiver's side. The clock is incorporated by the repetition code RTP and a start/stop code STP

Item (a) demands shunt termination though driving with current sources. Item (b) secures the data transmitted between the ICs by minimizing EM radiation. No data dependent peripheral supply consumption will occur. Furthermore, the bus can be put in idle mode that minimized power consumption effectively. Asynchronous modes are allowed as the clock is embedded with the data. Item (c) and (d) rule out the positive signal supply which leaves V_{TT} as the current-less termination potential. Combined with (a) this allows a signal swing between ground and the output supply, which is consistent with (c). As an added benefit, this simplifies CMOS differential receivers because they need simple N- and P-transistors of which their V_T-s are used as threshold level compared to V_{TT}. Item (e) allows asynchronous interface designs as the clock is embedded with the data by a repetition code.

Higher-level data organization is outside of the scope of this specification, though it should be noted that variations in the peripheral supply and ground current are unlikely to occur with this protocol even at maximum performance due to its coding. For this reason, I^2Q is intended for use with other DC-balanced data groupings such as 4B/6B and differential (1B/2B) codes.

Specific applications are also outside of this specification's scope. That said, it should be noted that the idle mode greatly simplifies hot-insertion systems.

4B-4T IC Interconnect standard (Inter IC Quad wire bus: I^2Q)

1. Scope

This standard defines the input, output, and termination specifications for differential signaling in the I^2Q environment, nominally between 0 and 2,5 V while maintaining constant supply current during operation. Power supplies other than the nominal 2,5 V power for the I^2Q interface are not specified but possible.

2. Description

I^2Q is a balanced coded differential current driven but voltage-based signaling protocol. The nominal low level; V_{OL} (ground), the intermediate level; V_{TT} 1,25 V and a nominal high level; V_{OH} of 2,5 V are defined.

Because the driver impedance must be matched to the line and termination impedances, this requires a nominal 2,5 V peripheral power supply (VDDQ). I^2Q defines three primitive types: drivers, receivers and terminators. A practical I^2Q system must have at least one of each type, although it is possible and in fact quite practical for all three to be located at separate nodes (to allow bus structures). For point-to-point connections, these types may be incorporated into a single node.

This inter-IC communication concept is registered as PHNL030102EPP: "Data communication using constant total current"

2.1 Drivers

Each individual line of an I^2Q driver is defined to be in one of three states, see figure 1:

- No voltage i.e. current drive:
  - The maximum output voltage will be V_{TT} (1,25 V) - V_T
- Medium voltage i.e. current drive:

- The output voltage will be V_{TT} (1,25 V)

- High voltage i.e. current drive:
  - The minimum output voltage will be V_{TT} (1,25 V) + V_T

In idle mode, the signal at the output of the driver will be {1, 1, 1, 1}. In this condition, the total current through the 4 output drivers can be ramped up, ramped down or kept constant without affecting the output signal, see figure 2.

2.2 Receivers

An I2Q receiver is defined to be in one of three states:

- The input voltage will be less or equal than V_{TT} (1,25 V) - V_T = "0"
- The input voltage will be about V_{TT} (1,25 V) = "1"
- The input voltage will be higher or equal than V_{TT} (1,25 V) + V_T = "2"

In idle mode, all four inputs are at {1, 1, 1, 1}

2.3 Terminators

Two options for I^2Q terminations are considered:

- Incorporated within the drivers, receivers when point-to-point interfaces are considered
- Separate from the drivers, receivers when a bi-directional bus concept is considered

In either case, the average power consumption by the termination of each line will be limited to:

$$1/3\ [(V_{DDQ} - V_{TT})^2/Z_0 + 0 + (V_{TT} - V_{SSQ})^2/Z_0)]$$

in active mode, assuming a homogeneous distribution of codes.

In idle case, the data i.e. output voltage is set to {1, 1, 1, 1} and no power is dissipated at the receiver's side. At the driver's side, the current can be made zero and the voltage can be set to V_{TT}, see figure 2.

3. Parametrics

I^2Q currents and impedances are specified in the context of odd-mode transmission-line impedances between 50 and 62 Ω (56 Ω ± 10%). In the interest of standardization, implementers should attempt to conform to this range. For lower or higher

line impedances, the currents specified herein should be scaled to satisfy the receiver's voltage requirement conditions.

When the terminations are integrated with the drivers, receivers for point-to-point applications, the characteristic line impedance requirement shall be met and matched with the other lines of the interface.

The crosstalk between the four individual lines of the I^2Q interface (or multiples thereof) shall be made less than 10% for each code of occurrence by proper transmission line topologies. The length i.e. propagation delay of each line of the I^2Q interface shall be chosen equal.

3.1 Power Supply

I^2Q uses only one peripheral power supply. V_{TT} shall be generated at each driver and receiver's side as voltage reference for the ternary level. With bi-directional interfaces a single voltage reference can be used

3.2 Receiver parametrics

Although performance requirements dictate that I^2Q systems maintain balanced currents in both the driver and terminator devices

3.2.1 Receiver classes

Class I receivers compare have no propagation path correction.

NOTE In most cases, the maximum bit rate per I^2Q interface is restricted to 1 Gbit/s/wire.

Class II receivers compare have propagation path correction.

NOTE In this case, the minimum bit rate per I^2Q interface is at least 1 Gbit/s/wire.

3.3 Driver parametrics

I^2Q defines two classes of drivers.

- Class A drivers are intended for point-to-point operation, so the load seen by the driver is nominally Z_0. For these bi-directional applications, the driver, receiver and termination are incorporated in the devices.
- Class B drivers are intended for multi-drop bus operation; the load seen by them is $Z_0/2$. For these bi-directional applications, the driver, receiver is incorporated in the devices and the termination is dealt with externally.

The driver's current shall be adapted to the loading requirements. By circuit topology of the switched current sources, the resulting di/dt glitches on the peripheral supply current shall not exceed 10% of the nominal supply current of ≈180 mA.

3.3.1 Class A drivers

The typical transition time will be ≥ 0,3 ns. The skew in-between the 4 transitions shall be less than 0,1 ns.

NOTE: The output voltage must remain within the specified limits relative to V_{TT} for balanced loads of between 50 and 62 ohms to ground. In this case, one termination will be internal i.e. the same total current will be required as with class B drivers.

3.3.2 Class B drivers

The typical transition time will be « 0,3 ns. The skew in-between the 4 transitions shall be less than 0,05 ns.

NOTE: The output voltage must remain within the specified limits relative to V_{TT} for balanced loads of between 25 and 31 ohms to ground.

4. Protocol

For an I^2Q interface, the specification is reduced to a basic single channel of 4 bits/wires. It is expected that use of one or more independent 4-bit I^2Q channels can provide best data to clock skew performance, while 4-bit granularity also allows easy bus scaling.

The I^2Q specification for the interface can be summarised with the following rules:

1. Values of 4 binary bits are coded into balanced 4B4T code as given in the table 1 below
2. The bus is bi-directional: one agent drives, all other agents receive ("driving" code IDL)
3. While in power down or receive mode the bus is non driven (idle, code IDL)
4. Repetition of I^2Q bus (non-IDL) codes is eliminated by sending repeat code (RPT) instead
5. Receiving agents regenerate a data sampling clock from the I^2Q signal edges
6. A transaction is started by sending at least 8 stop/repeat codes (STP, RPT, etc)
7. A transactions is stopped by sending at least 8 stop codes (STP, RPT, etc)
8. During operation the I^2Q IO driver supply current modulation is compensated
9. Only one bus agent has bus control and is bus master at any time
10. Other agents can take over bus control and become master by token passing
11. A new bus master must wait for at least one bus IDL cycle before taking over
12. One default (reset) master module provides a frequency reference clock for all receivers
13. More I^2Q busses when working in parallel operate independently

14. Higher levels of protocol can be filled in according application (for the time being)

Table 1 Coding table for 4 binary bits to balanced 4B4T format

Function	Symbol	4B4T
Repeat	RPT	{2,1,0,1}
Stop	STP	{2,0,1,1}
Idle	IDL	{1,1,1,1}
"0000"	0x	{1,1,0,2}
"0001"	1x	{1,0,1,2}
"0010"	2x	{1,2,1,0}
"0011"	3x	{1,1,2,0}
"0100"	4x	{2,0,2,0}
"0101"	5x	{0,1,2,1}
"0110"	6x	{1,2,0,1}
"0111"	7x	{2,0,0,2}
"1000"	8x	{1,0,2,1}
"1001"	9x	{0,0,2,2}
"1010"	Ax	{0,2,1,1}
"1011"	Bx	{0,2,0,2}
"1100"	Cx	{2,1,1,0}
"1101"	Dx	{0,2,2,0}
"1110"	Ex	{0,1,1,2}
"1111"	Fx	{2,2,0,0}

The embodiments of the present invention described herein are intended to be taken in an illustrative and not a limiting sense. Various modifications may be made to these embodiments by those skilled in the art without departing from the scope of the present invention as defined in the appended claims.

CLAIMS:

1. A data communication system, comprising:

- at least three signal conductors;

- a first and second power supply terminal, for supplying currents of mutually opposite direction to the signal conductors respectively;

- a driver circuit coupled between the power supply terminals and the signal conductors, the driver circuit being arranged to establish a combination of currents through respective ones of the signal conductors, the driver circuit selecting successive combinations, dependent on information to be transmitted, from a selectable set of combinations, at least three different levels of current to any signal conductor being used in the set, including a current level of current to the signal conductors from the first power supply and a current level of current from the signal conductors to the second power supply, a sum of the currents through the signal conductors substantially having a same value for each combination in the set and at least one of the conductors not merely functioning in a differential pair relation with another one of the conductors.

2. A method communication data via at least three signal conductors, the method comprising:

- using currents of mutually opposite polarity from a first and second power supply terminal respectively to establish successive combinations of currents on respective ones of the signal conductors, the combinations being selected dependent on information to be transmitted, so that a sum of the currents through the signal conductors substantially has a same value for each combination and at least one of the conductors functioning does not merely function in a differential pair relation with another one of the conductors, at least three different levels of current to any signal conductor being used in the set of selectable combinations, including a current level of current to the signal conductors from the first power supply and a current level of current from the signal conductors to the second power supply.

ABSTRACT:

A data communication system, comprising has at least three signal conductors and a first and second power supply terminal, for supplying currents of mutually opposite direction to the signal conductors respectively. A driver circuit establishes respective combinations of currents through the signal conductors from a selectable set of combinations, which includes combinations with currents from the first supply terminal and to the second supply terminal, so that a sum of the currents through the signal conductors substantially has a same value for each combination and at least one of the conductors functioning does not merely function in a differential pair relation with another one of the conductors, the driver circuit determining which of the combinations from the set are established dependent on information to be transmitted.

Fig. 1